FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP035.C3	08/990,414
APPLICANT: Garg *et al.*	
FILING DATE: December 15, 1997	GROUP: 2783

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,901,233	02/1990	Liptay	395	375	
	AB1	4,903,196	02/1990	Pomerene *et al.*	364	200	
	AC1	4,942,525	07/1990	Shintani *et al.*	395	375	
	AD1	4,992,938	02/1991	Cocke *et al.*	364	200	
	AE1	5,067,069	11/1991	Fite *et al.*	395	375	
	AF1	5,109,495	04/1992	Fite *et al.*	395	375	
	AG1	5,142,633	08/1992	Murray *et al.*	395	375	
	AH1	5,214,763	05/1993	Blaner *et al.*	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1	O 515,166	11/1992	EP			Yes No
	AM1	O 533,337	03/1993	EP			Yes No
	AN1	WO 91/20,031	12/1991	WO			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	"Critical Issues Regarding HPS, A High Performance Microarchitecture", Yale N. Patt, Stephen W. Melvin, Wen-Mei Hwu and Michael C. Shebanow; The 18th Annual Workshop on Microprogramming, Pacific Grove, California, Dec. 3-6, 1985, IEEE Computer Order No. 653, pp. 109-116.
	AS	1	"HPS, A New Microarchitecture: Rationale and Introduction", Yale N. Patt, Wen-Mei Hwu and Michael C. Shebanow; The 18th Annual Workshop on Microprogramming, Pacific Grove, California, Dec. 3-6, 1985; IEEE Computer Society Order No. 653, pp. 103-108.
	AT	1	Peleg *et al.*, "Future Trends in Microprocessors: Out-Of-Order Execution, Spec. Branching and Their CISC Performance Potential", March 1991.
	AU	1	Lightner *et al.*, "The Metaflow Architecture", pp. 11-12, 63-68, IEEE Micro Magazine, June 1991.
	AV	1	John L. Hennessy & David A Patterson, Computer Architecture A Quantitative Approach, Ch. 6.4, 6.7 and pg. 449, 1990.

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	AA2	5,222,244	06/1993	Carbine *et al.*	395	800	
	AB2	5,226,126	07/1993	McFarland *et al.*	395	375	
	AC2	5,251,306	10/1993	Tran	395	375	
	AD2	5,261,071	11/1993	Lyon	395	425	
	AE2	5,345,569	09/1994	Tran	395	375	
	AF2	5,398,330	03/1995	Johnson	395	375	
	AG2	5,487,156	01/1996	Popescu *et al.*	395	375	
	AH2	5,355,457	10/1994	Shebanow *et al.*	395	375	

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2	0 378 195 A3	07/1990	EP			Yes No
	AM2						Yes No
	AN2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	2	Hwu, Wen-mei, Steve Melvin, Mike Shebanow, Chein Chen, Jia-juin Wei, Yale Patt, "An HPS Implementation of VAX: Initial Design and Analysis", Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences, pp. 282-291, 1986.
AS	2	Hwu *et al.*, "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers", COMPCON 86, 1986.
AT	2	Hwu, Wen-mei and Yale N. Patt, "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality", Proceedings of the 18th International Symposium on Computer Architecture, pp. 297-306, June 1986.
AU	2	Yale N. Patt, Stephen W. Melvin, Wen-mei Hwu, Michael C. Shebanow, Chein Chen, Jiajuin Wei, "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream", Proceedings of MICRO 19 Workshop, New York, New York, pp. 1-7, October, 1986.
AV	2	Swenson, John A. and Yale N. Patt, "Hierarchical Registers for Scientific Computers", St. Malo '88, University of California at Berkeley, pp. 346-353, 1988.

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	AA3	5,497,499	03/1996	Garg *et al.*	395	800	
	AB3	5,448,705	09/1995	Nguyen *et al.*	395	375	
	AC3						
	AD3						
	AE3						
	AF3						
	AG3						
	AH3						

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	AL3						Yes No
	AM3						Yes No
	AN3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Butler, Michael and Yale Patt, "An Improved Area-Efficient Register Alias Table for Implementing HPS", University of Michigan, Ann Arbor, Michigan, pp. 1-15, January, 1990.
	AS	3	Uvieghara, G.A., W.Hwu, Y. Nakagome, D.K. Jeong, D. Lee, D.A. Hodges, Y. Patt, "An Experimental Single-Chip Data Flow CPU", Symposium on ULSI Circuits Design Digest of Technical Papers, May, 1990.
	AT	3	Melvin, Stephen and Yale Patt, "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques", Proceedings From ISCA-18, pp. 287-296, May, 1990.
	AU	3	Butler, Michael, Tse-Yu Yeh, Yale Patt, Mitch Alsup, Hunter Scales and Michael Shebanow, "Single Instruction Stream Parallelism Is Greater Than Two" Proceedings of ISCA-18, pp. 276-286, May, 1990.
	AV	3	Uvieghara, Gregory A., Wen-mei, W. Hwu, Yoshinobu Nakagome, Deog-Kyoon Jeong, David D. Lee, David A. Hodges and Yale Patt, "An Experimental Single-Chip Data Flow CPU", IEEE Journal of Solid-State Circuits, Vol. 27, No. 1, pp. 17-28, January, 1992.

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	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	4	Gee, Jeff, Stephen W. Melvin, Yale N. Patt, "The Implementationof Prolog via VAX 8600 Microcode", Proceedings of Micro 19, New York City, PP. 1-7, October, 1986.
	AS	4	Hwu, Wen-mei Hwu and Yale N. Patt, "Design Choices for the HPSm Microprocessor Chip", Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences, pp. 330-336, 1987.
	AT	4	Wilson, James E., Steve Melvin, Michael Shebanow, Wen-mei Hwu and Yale N. Patt, "On Turning the Microarchitecture of an HPS Implementation of the VAX", Proceedings of Micro 20, pp. 162-167, December, 1987.
	AU	4	Hwu, Wen-mei and Yale N. Patt, "HPSm2: A Refined Single-chip Microengine", HICSS '88, pp. 30-40, 1988.
	AV	4	Keller, "Look-Ahead Processors"; Dec. 1975, pp. 177-194.

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	AA5						
	AB5						
	AC5						
	AD5						
	AE5						
	AF5						
	AG5						
	AH5						

FOREIGN PATENT DOCUMENTS

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	AL5						Yes No
	AM5						Yes No
	AN5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	5	Dywer, A Multiple, Out-of-Order, Instruction Issuing System For SuperScaler Processors, (All); Aug. 1991.
	AS	5	Lightner *et al.*, "The Metaflow Lightning" Chip Set Mar. 1991 *IEEE Lightning Outlined. Microprocessor Report* Sep. 1990.
	AT	5	Michael D. Smith *et al.*, "Limits on Multiple Instruction Issue," Computer Architecture News, No. 2, April 17, 1989, pp. 290-302.
	AU	5	Gurindar S. Sohi *et al.*, "Instruction Issue Logic for High Performance, Interruptable Pipelined Processors," *The 14th Annual International Symposium on Computer Architecture*, June 2-5, 1987, pp. 27-34.
	AV	5	

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